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U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

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APPL NUM 10016449	FILING DATE 12/10/2001	CLASS 714	SUBCLASS 725	GAU 2133	EXAMINER <i>Jabone</i>
**APPLICANTS: Bailis Robert; Kuhlmann Charles; Lingafelt Charles; Rincon Ann; <i>RKD</i>					
**CONTINUING DATA VERIFIED:					
** FOREIGN APPLICATIONS VERIFIED:					
PG-PUB <input type="checkbox"/> DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>			
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no		35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO	
Verified and Acknowledged Examiners's initials		RPS920010127US1			
TITLE : Method and system for use of a field programmable gate array (FPGA) function within an application specific integrated circuit (ASIC) to enable creation of a debugger client within th <small>U.S. DEPT. OF COMM./PAT. & TM.-PTO-426L (Rev. 12-94)</small>					

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Assistant Examiner	
ISSUE FEE		Total Claims	
Amount Due	Date Paid	Print Claim for O.G.	
		DRAWING	
		Sheets Drwg.	Figs. Drwg.
		Print Fig.	
		Primary Examiner	
<input type="checkbox"/> TERMINAL DISCLAIMER		Application Examiner	
		PREPARED FOR ISSUE	
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